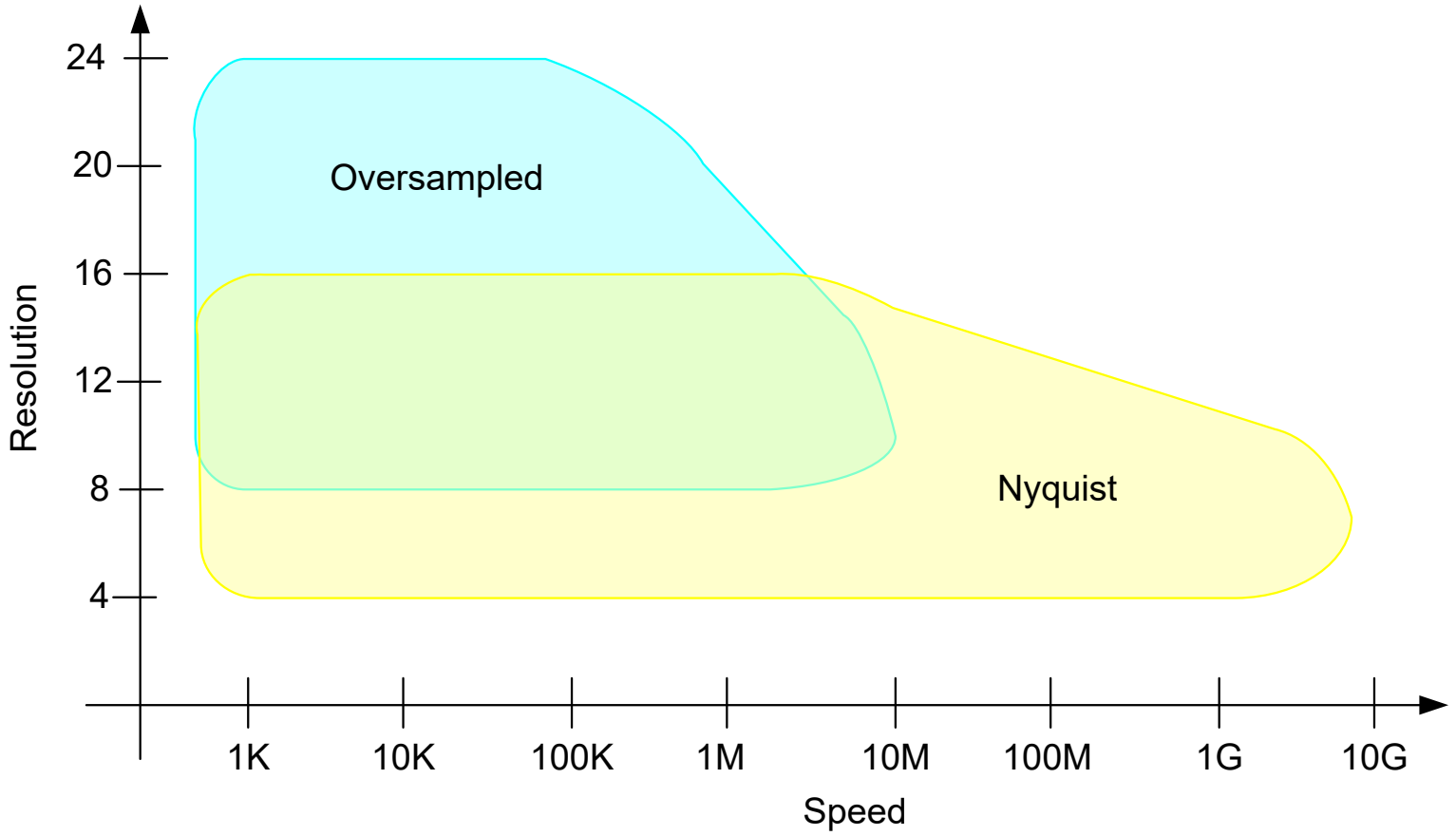
EE 435

Lecture 39

ADC Design

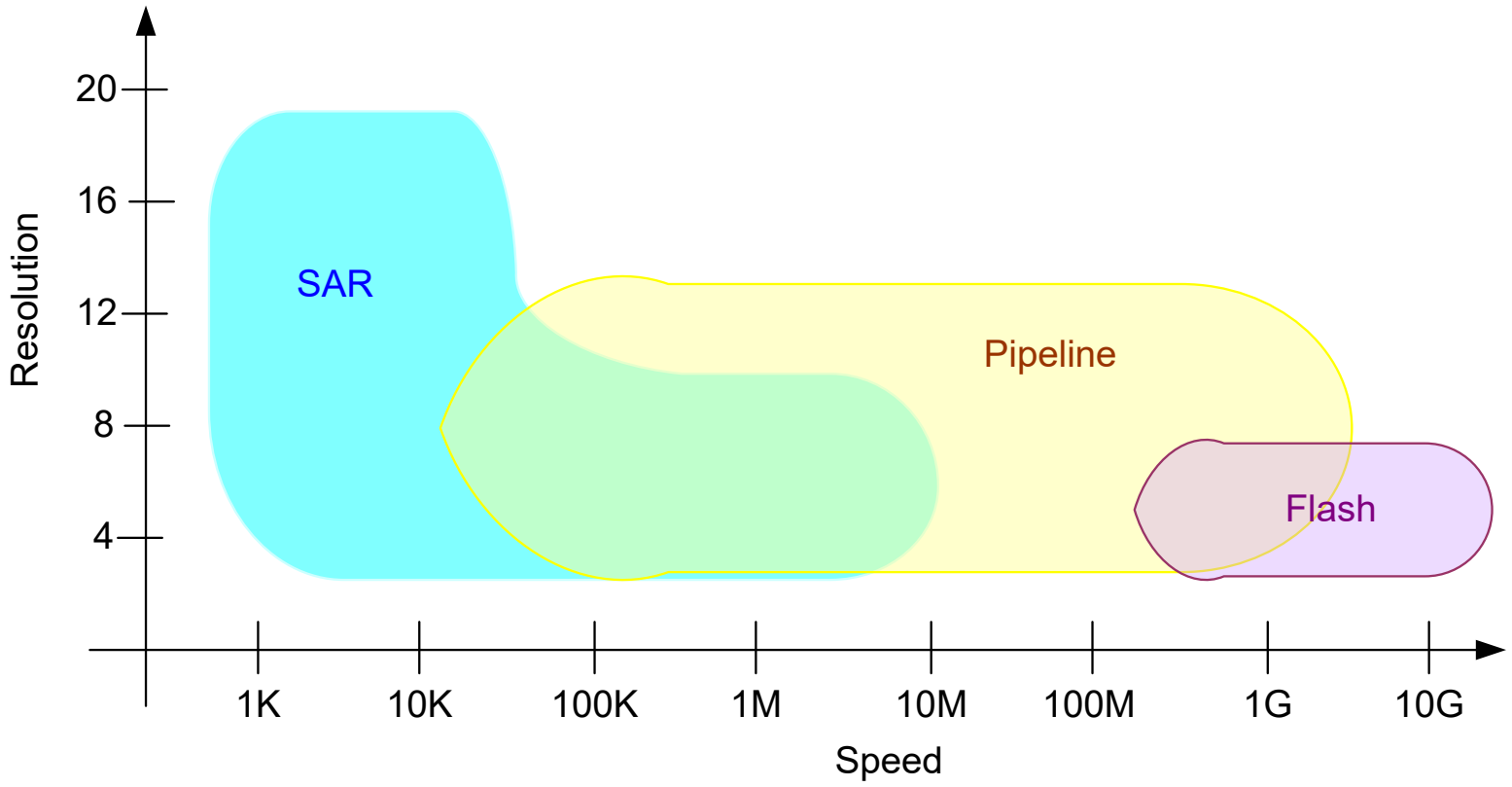
Review from Last Lecture

Data Converter Type Chart



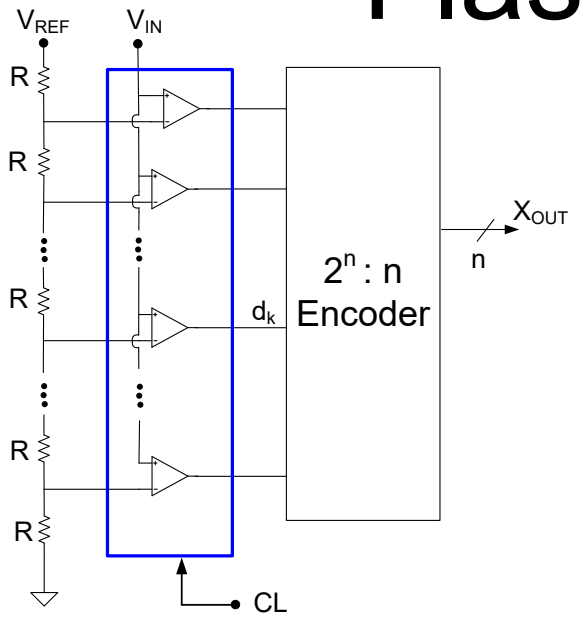
Review from Last Lecture

Nyqyist Rate Usage Structures



Review from Last Lecture

Flash ADC



Asynchronous operation (benefit or liability?)
Vulnerable to missing codes
High number of comparators needed (for large n)
R-string area requires considerable area and source of INL limitations
Offset voltage of comparators of concern
Simultaneous switching of large number of comparators can cause supply glitches
Large parasitic capacitance on V_{IN} pin
Bubbles in output can occur
Metastability an issue
Power dissipation can be large

Flash ADC Summary

Flash ADC

- Very fast
- Simple structure
- Usually Clocked
- Bubble Removal Important
- Seldom over 6 or 7 bits of resolution

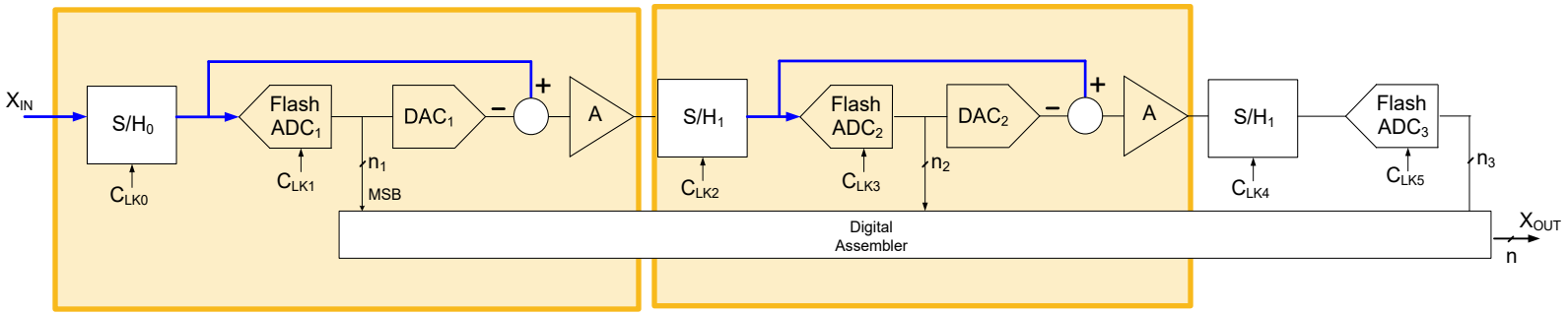
  - Flash ADC has some really desirable properties (simple and fast)
  - Wouldn't it be nice if we could derive most of the benefits of the FLASH ADC without the major limitations

To be practical at higher resolution, must address the major limitation of the FLASH ADC

Major Limitation of FLASH ADC at higher resolutions?

Number of comparators increases geometrically --- 2^n

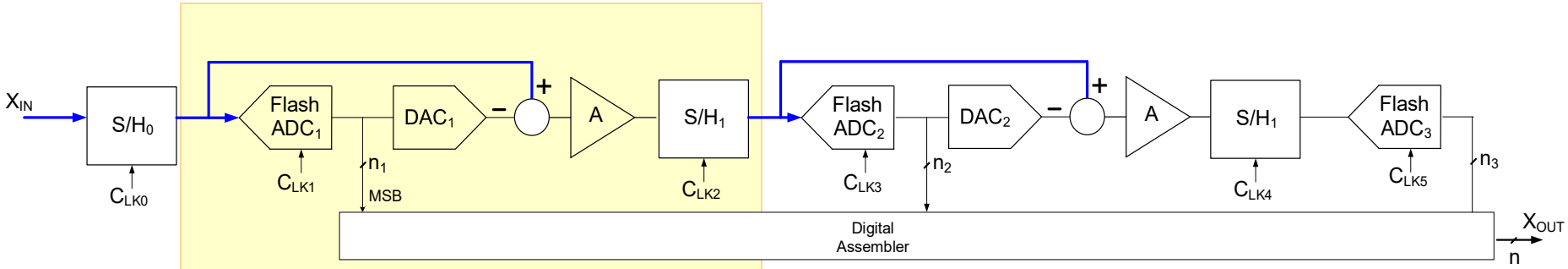
Three-Step Flash ADC with Interstage Gain and S/H

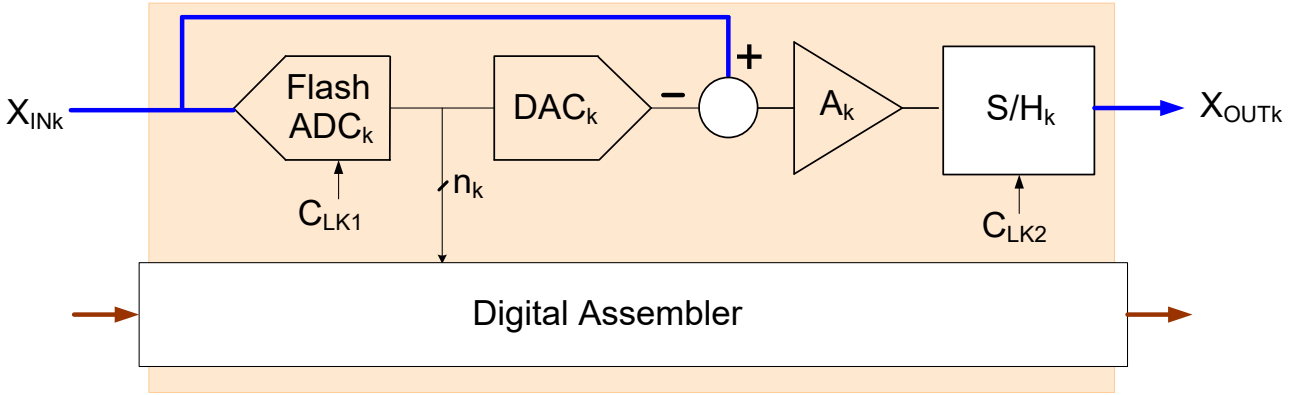


- Further reduces number of comparators needed!
- Even more complexity!
- But appears first two stages perform identical operations (if $n_1=n_2$)
- S/H$_1$ frees first stage to take another sample during second stage conversion
- S/H$_2$ frees second stage to take another sample during third stage conversion
- **This has a pipelining capability !**

Review from Last Lecture

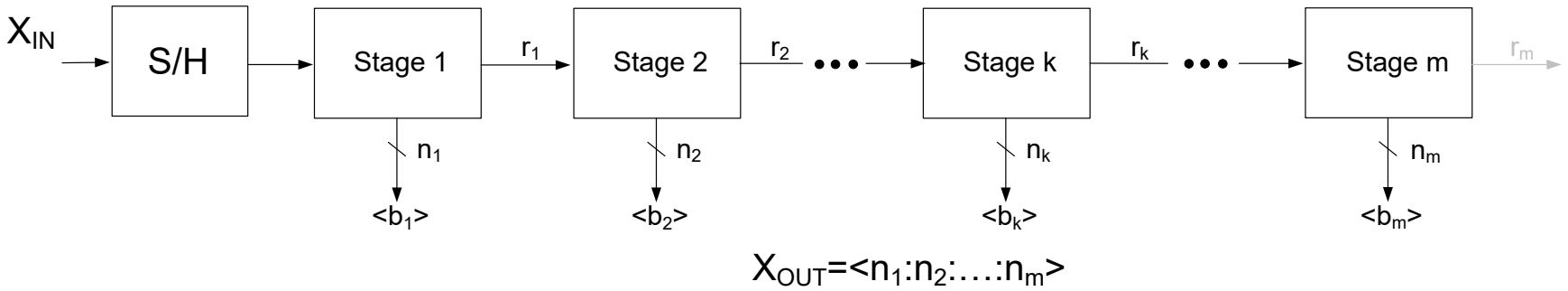
Three-Step Flash ADC with Interstage Gain



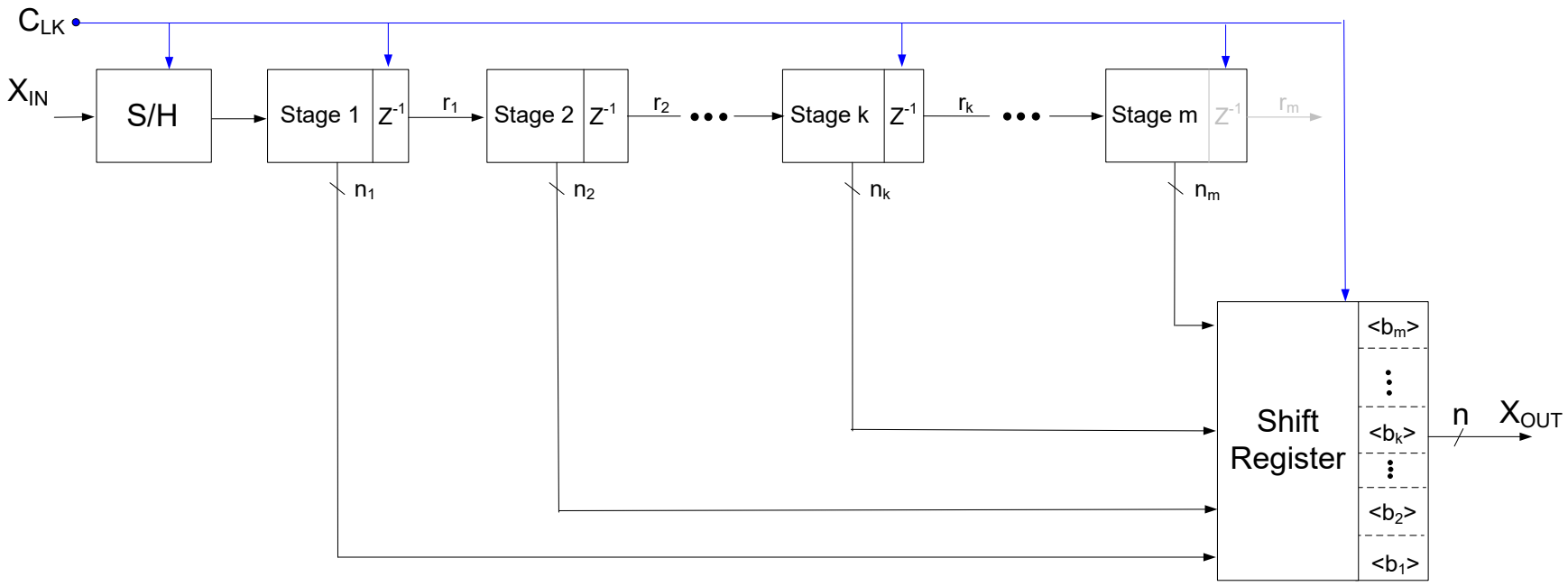


Review from Last Lecture

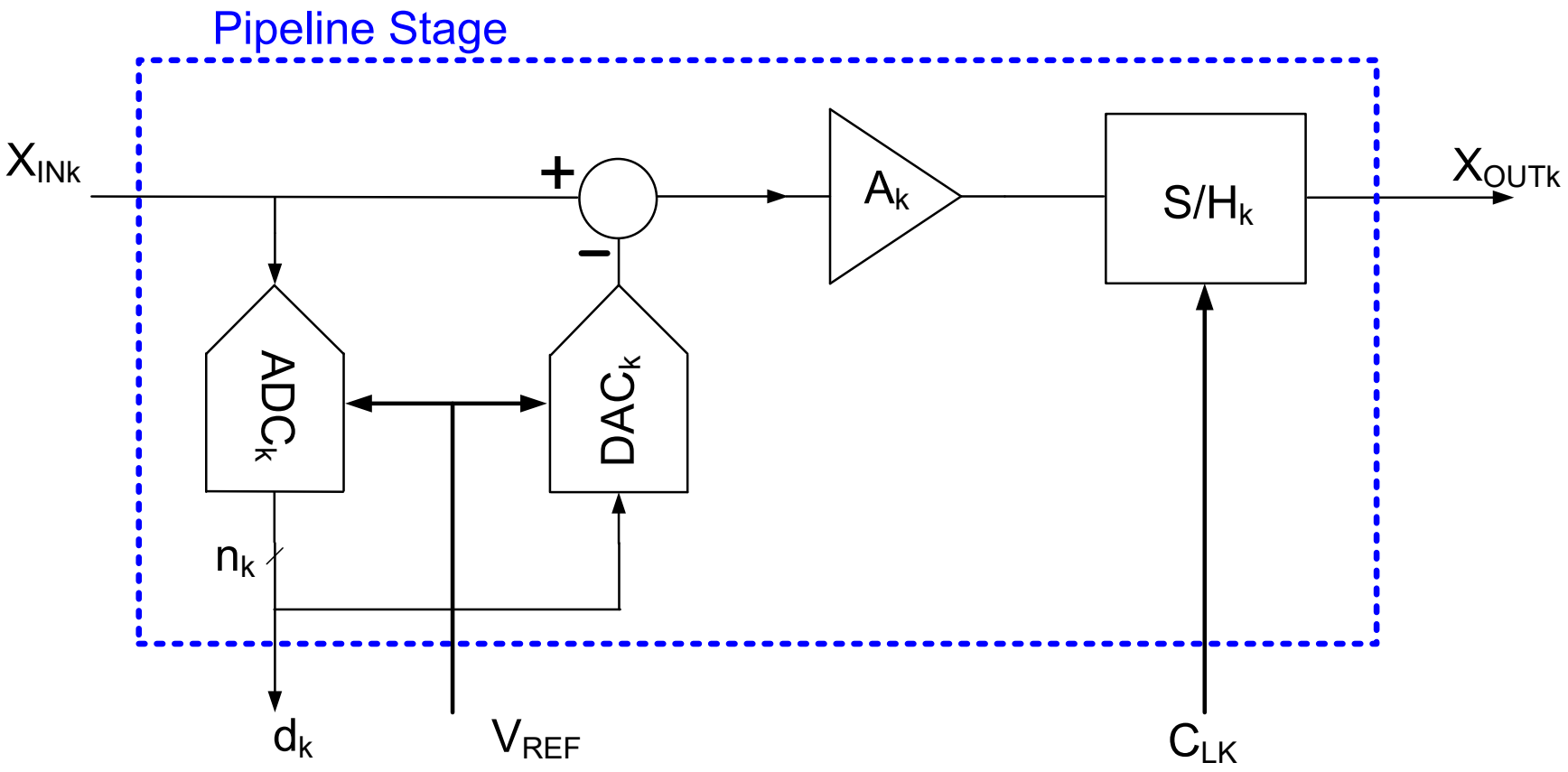
Pipelined ADC



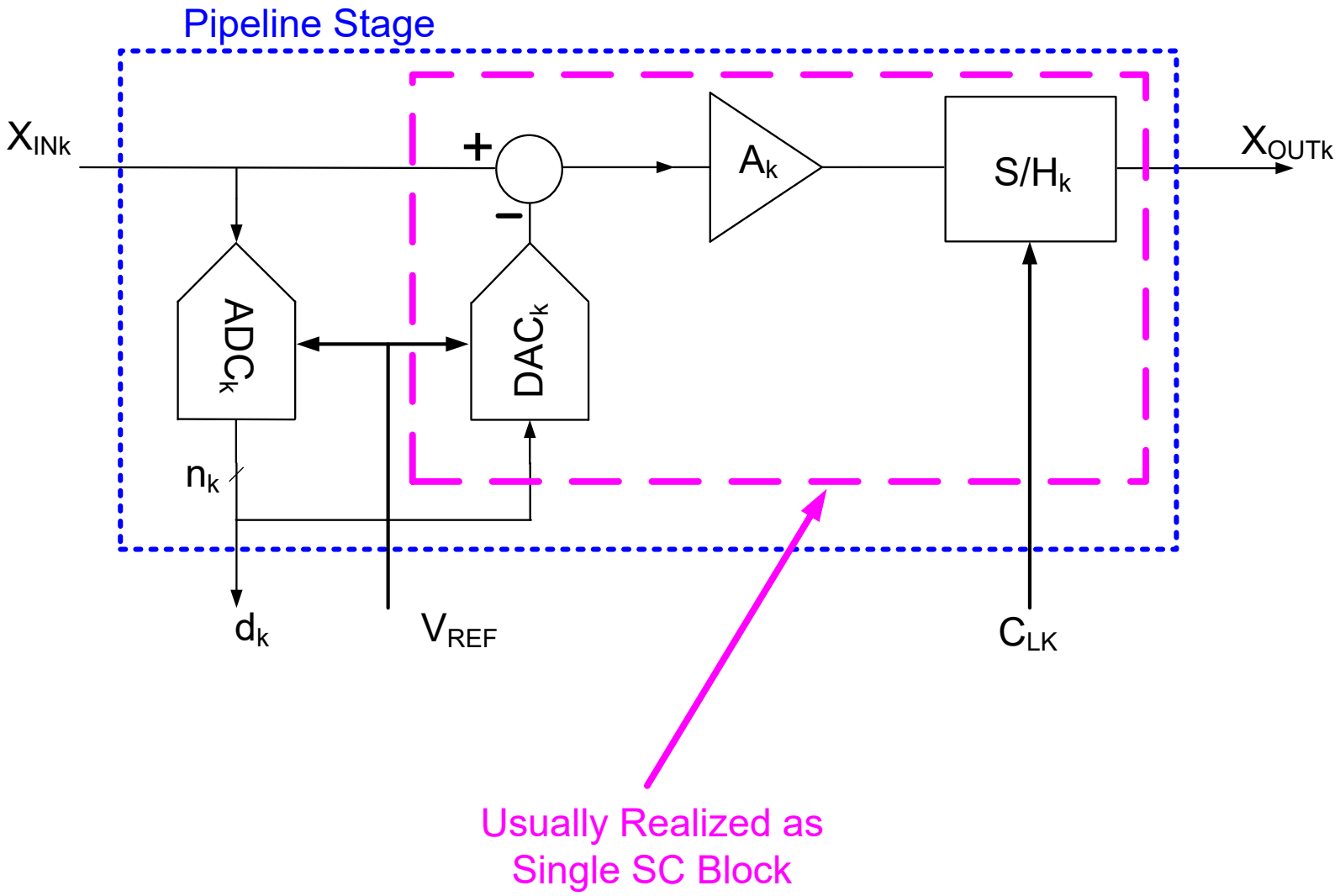
Pipelined ADC



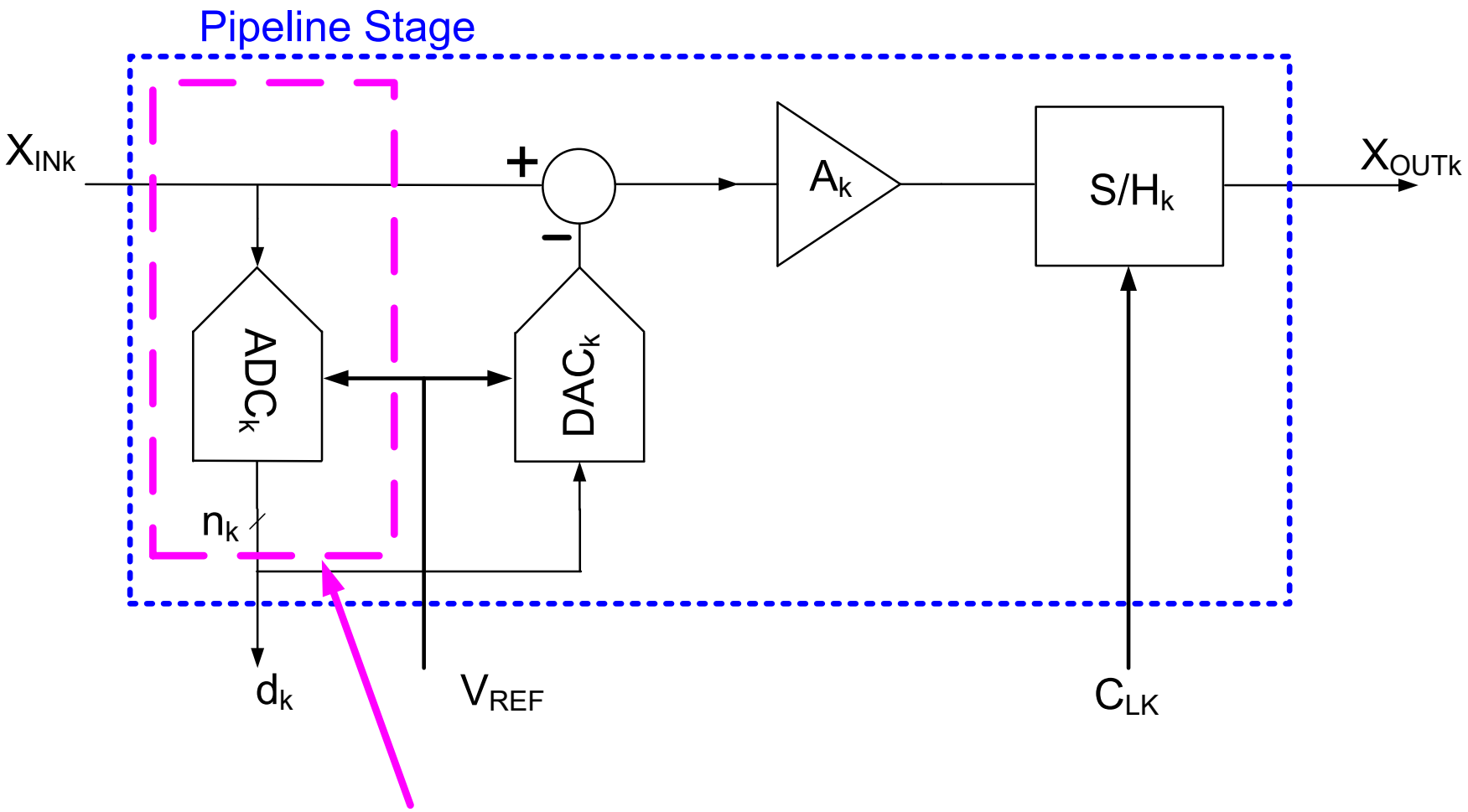
Pipelined ADC Stage k



Pipelined ADC Stage k

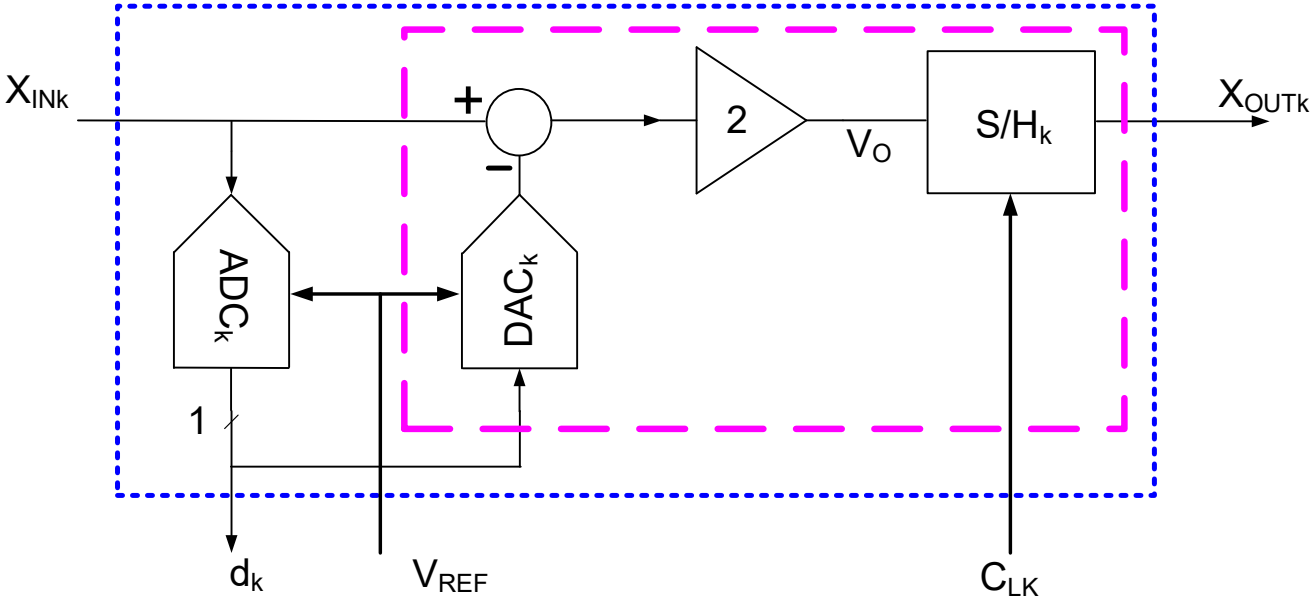


Pipelined ADC Stage k



Pipelined ADC Stage k

Pipeline Stage for 1 bit/stage

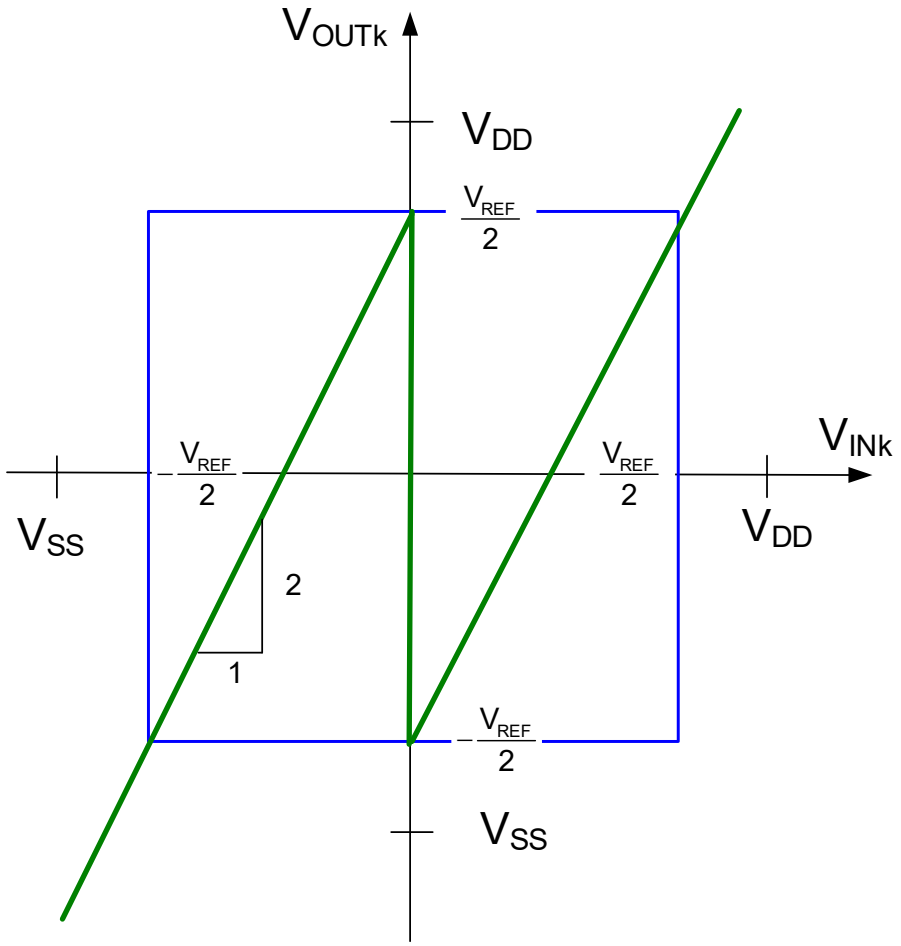


Assuming $-\frac{V_{REF}}{2} < V_{IN_k} < \frac{V_{REF}}{2}$

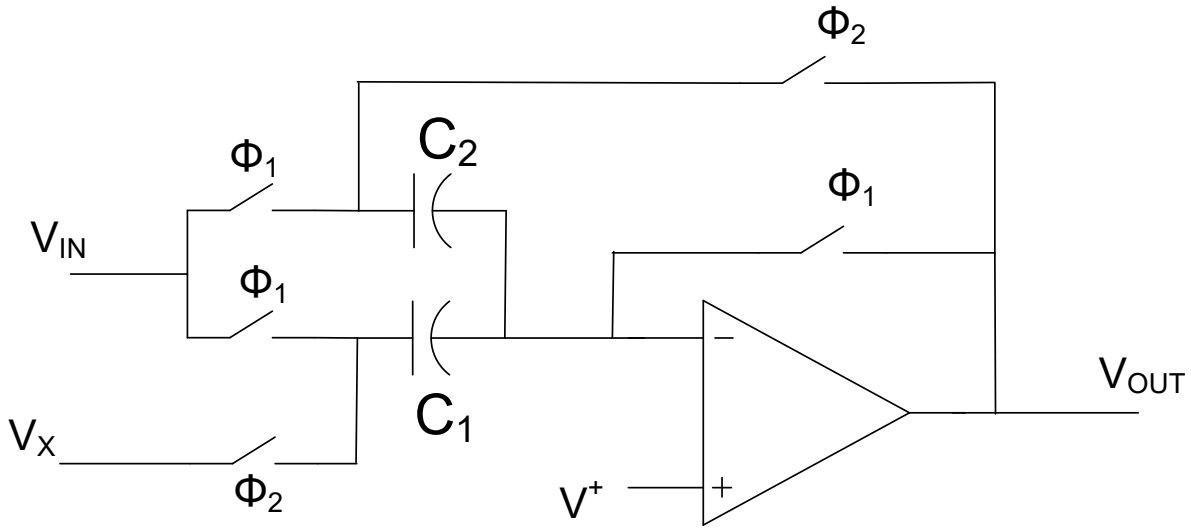
$$V_{Ok} = \begin{cases} 2V_{IN_k} + \frac{V_{REF}}{2} & V_{IN_k} < 0 \\ 2V_{IN_k} - \frac{V_{REF}}{2} & V_{IN_k} > 0 \end{cases}$$

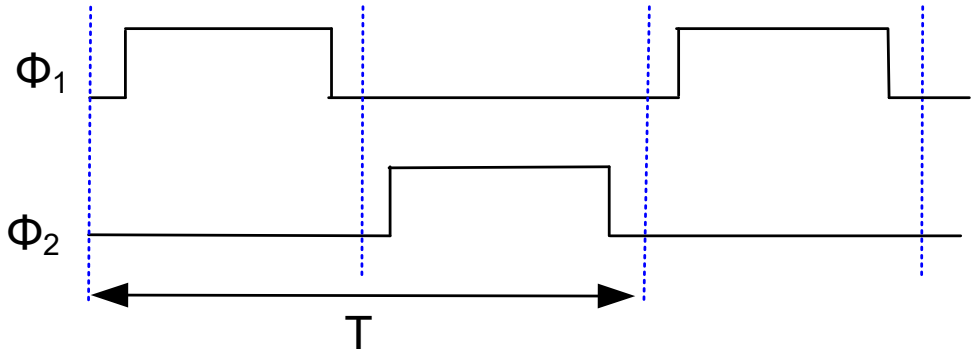
Transfer Characteristics for 1 bit/stage

$$V_{O_k} = \begin{cases} 2V_{IN_k} + \dfrac{V_{REF}}{2} & V_{IN_k} < 0 \\ 2V_{IN_k} - \dfrac{V_{REF}}{2} & V_{IN_k} > 0 \end{cases}$$



Consider the following circuit





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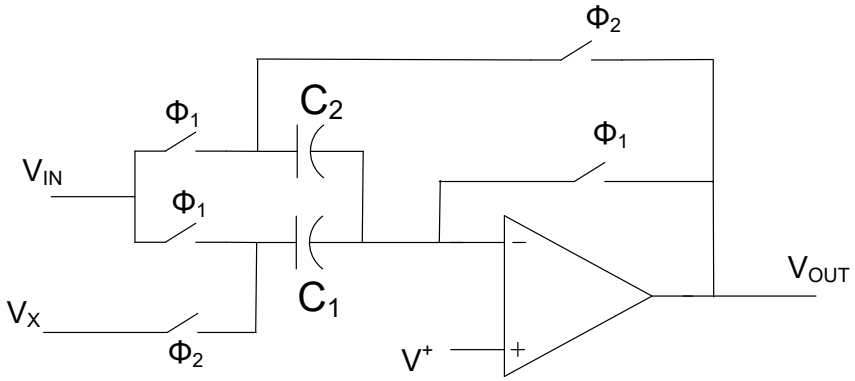
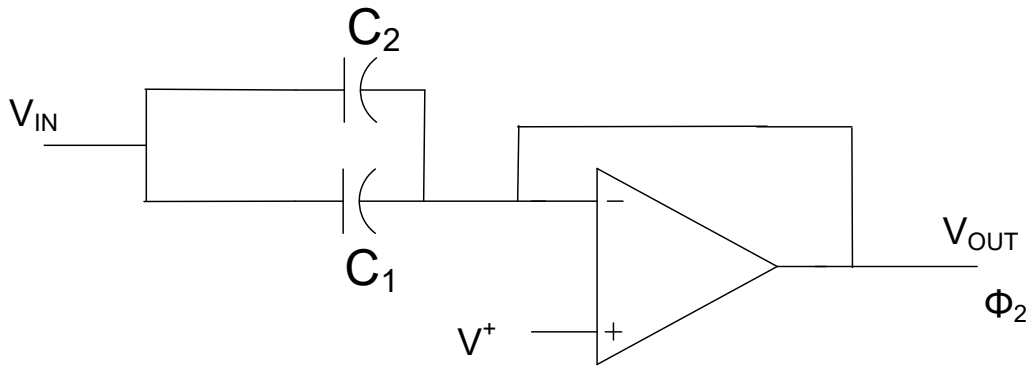


During Φ_1



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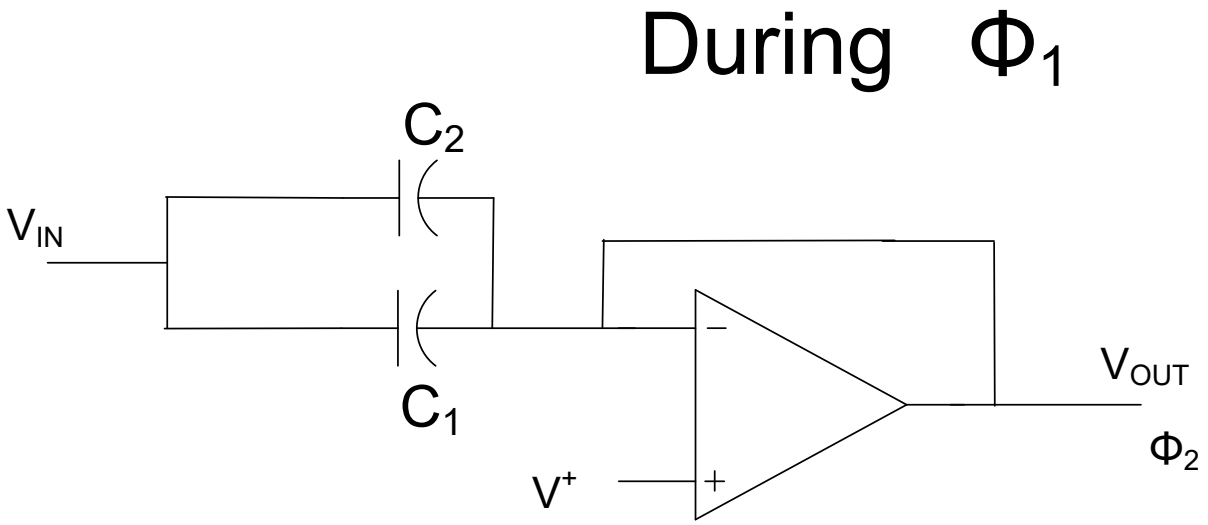
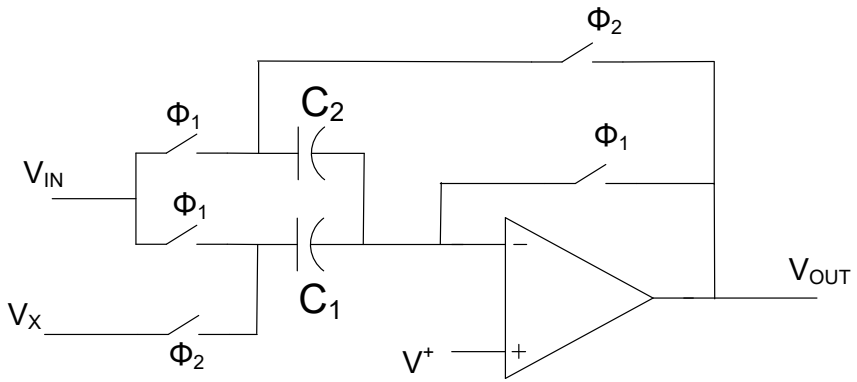
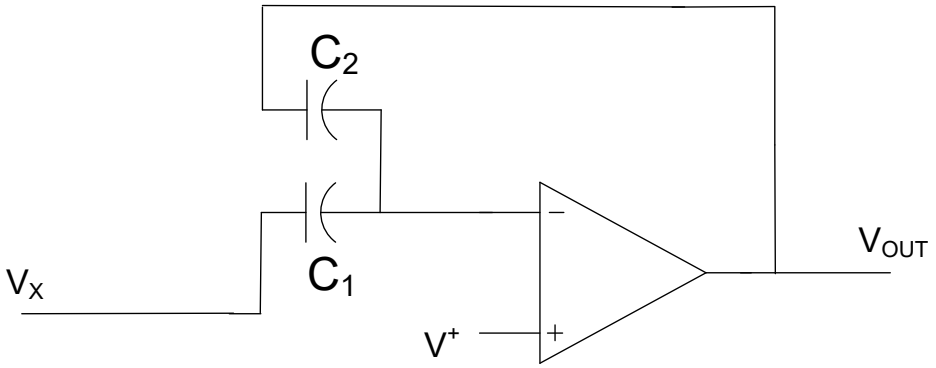


$$Q_1 = C_1\left(V_{IN} - V^+\right)$$
$$Q_2 = C_2\left(V_{IN} - V^+\right)$$

Consider the following circuit



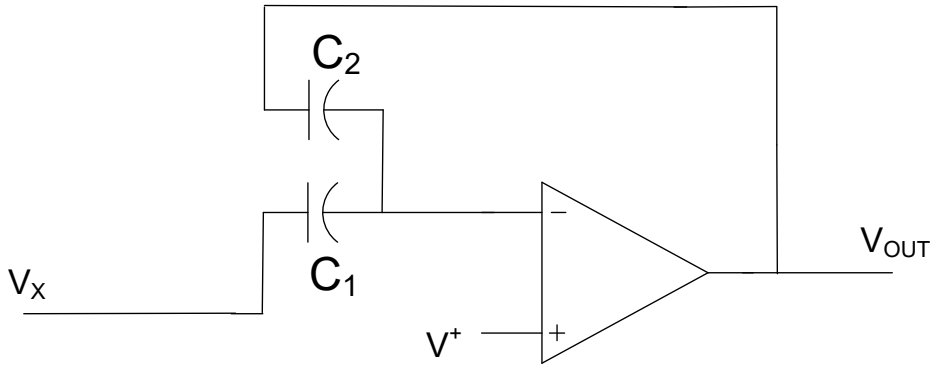
During Φ_2



Consider the following circuit

$$Q_1 = C_1\left(V_{IN} - V^+\right)$$
$$Q_2 = C_2\left(V_{IN} - V^+\right)$$

During Φ_2



Define Q_{1T} to be the charge transferred from C_1 during phase Φ_2

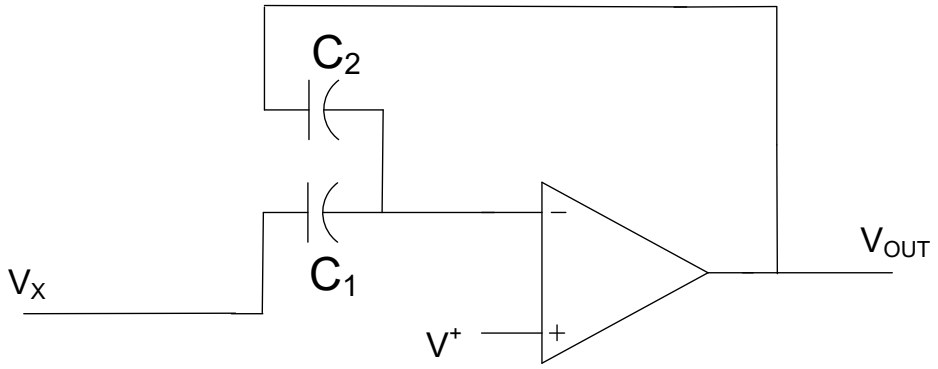
$$Q_{1T} = C_1\left(V_{IN} - V^+\right) - C_1\left(V_X - V^+\right) = C_1\left(V_{IN} - V_X\right)$$

Define Q_{2F} to be the total charge on C_2 during phase Φ_2

$$Q_{2F} = Q_2 + Q_{1T} = C_2\left(V_{IN} - V^+\right) + C_1\left(V_{IN} - V_X\right) = \left(C_1 + C_2\right)V_{IN} - C_2V^+ - C_1V_X$$

Consider the following circuit

During Φ_2

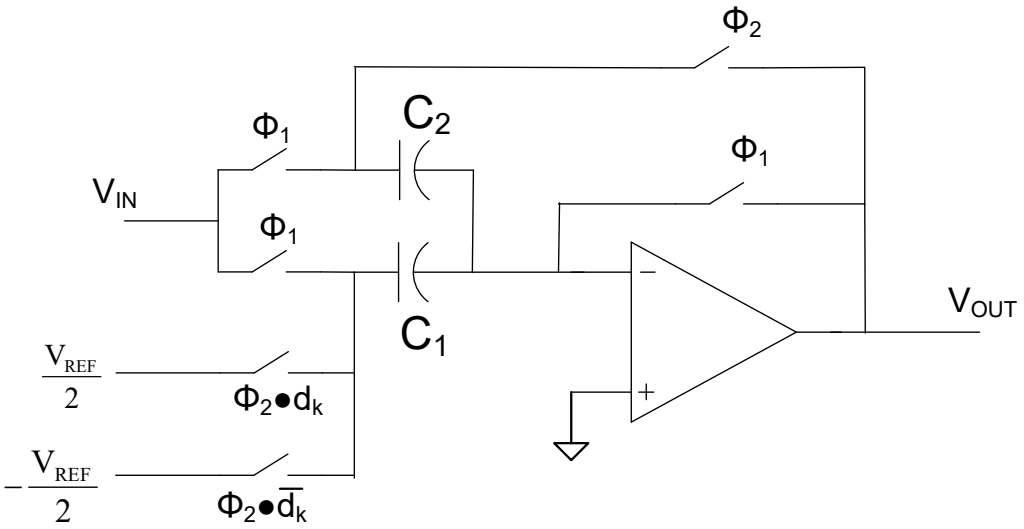


$$Q_{2F} = (C_1 + C_2)V_{IN} - C_2V^+ - C_1V_X$$

$$V_{C2F} = \frac{Q_{2F}}{C_2} = \left(1 + \frac{C_1}{C_2}\right)V_{IN} - V^+ - \frac{C_1}{C_2}V_X$$

$$V_{OUTF} = V_{C2F} + V^+ = \left(1 + \frac{C_1}{C_2}\right)V_{IN} - \frac{C_1}{C_2}V_X$$

Consider the following circuit

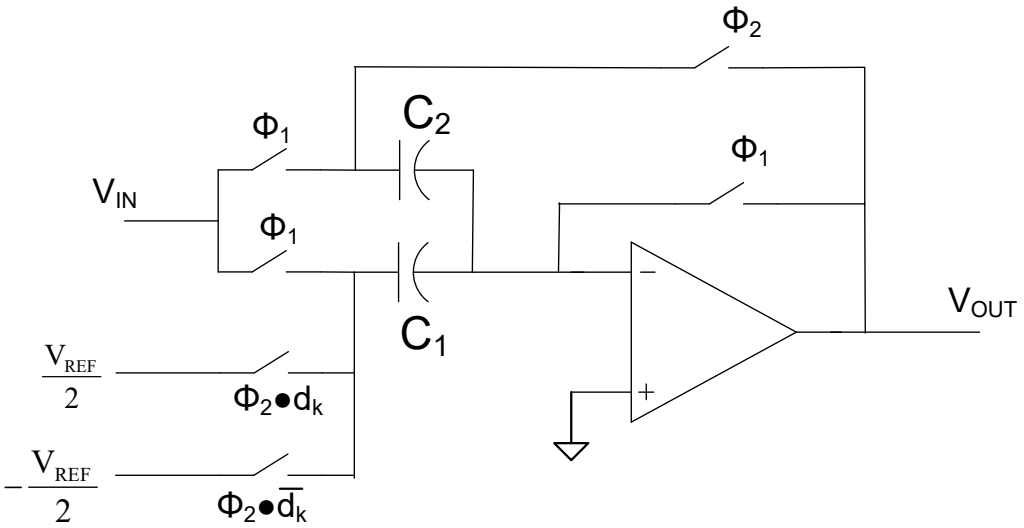


$$V_{OUTF} = \left(1 + \frac{C_1}{C_2}\right) V_{IN} - \frac{C_1}{C_2} V_X$$

If $C_1 = C_2 = C$ and $V_X = -\frac{V_{REF}}{2}$

$$V_{OUTF} = 2V_{IN} + \frac{V_{REF}}{2}$$

Consider the following circuit



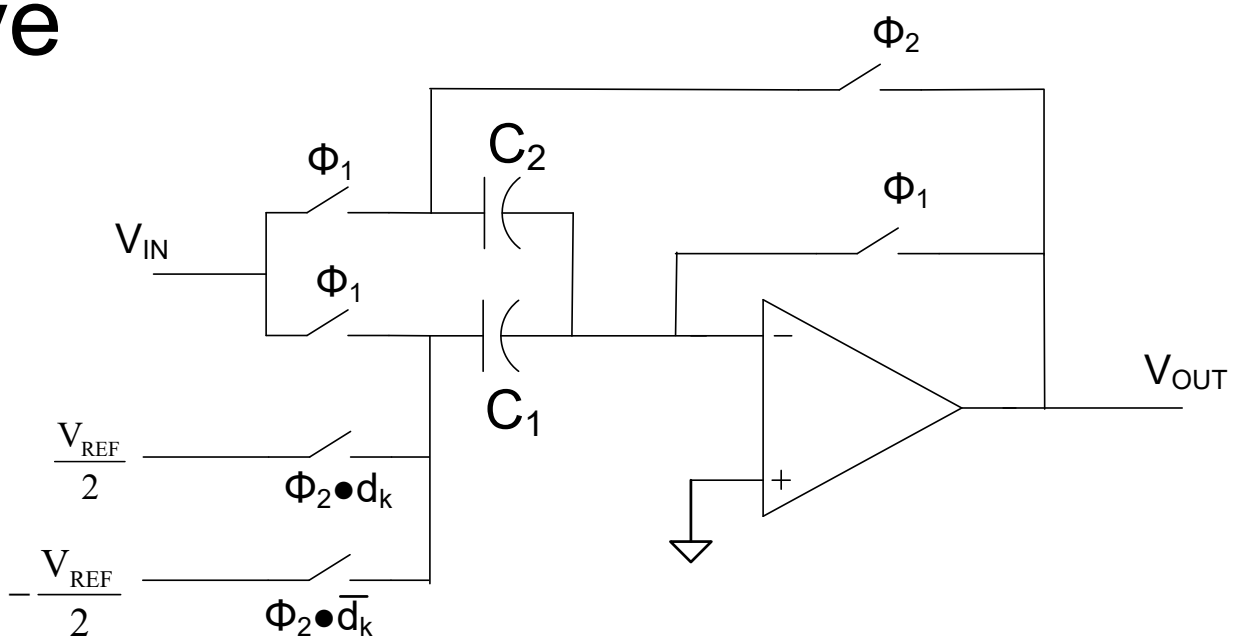
$$V_{OUTF} = \left(1 + \frac{C_1}{C_2}\right) V_{IN} - \frac{C_1}{C_2} V_X$$

Likewise

If $C_1 = C_2 = C$ and $V_X = \frac{V_{REF}}{2}$

$$V_{OUTF} = 2V_{IN} - \frac{V_{REF}}{2}$$

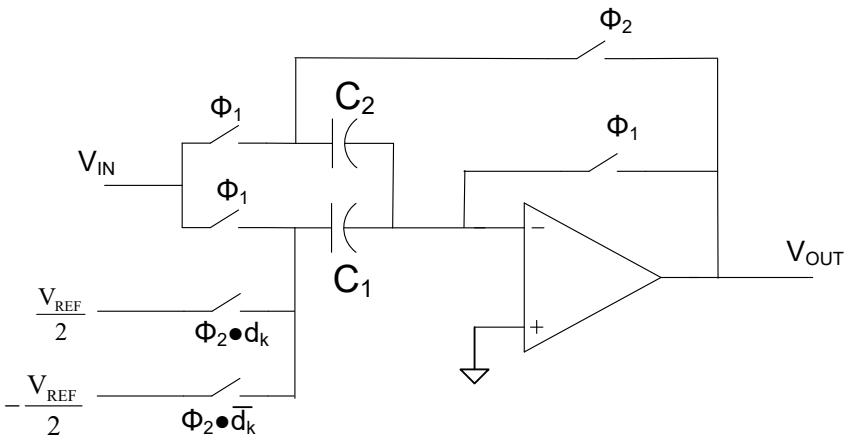
Observe

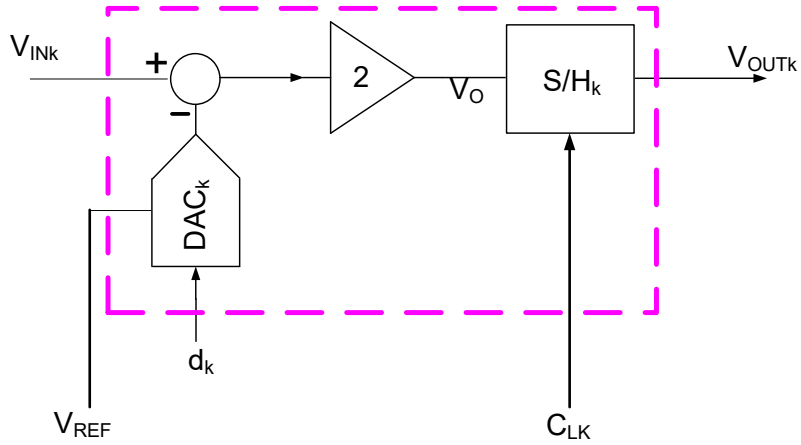


$$V_O = \begin{cases} 2V_{IN} + \dfrac{V_{REF}}{2} & V_{IN} < 0 \\ 2V_{IN} - \dfrac{V_{REF}}{2} & V_{IN} > 0 \end{cases}$$

This is exactly what is needed for the transfer characteristics needed for each stage in a 1 bit/stage pipelined ADC

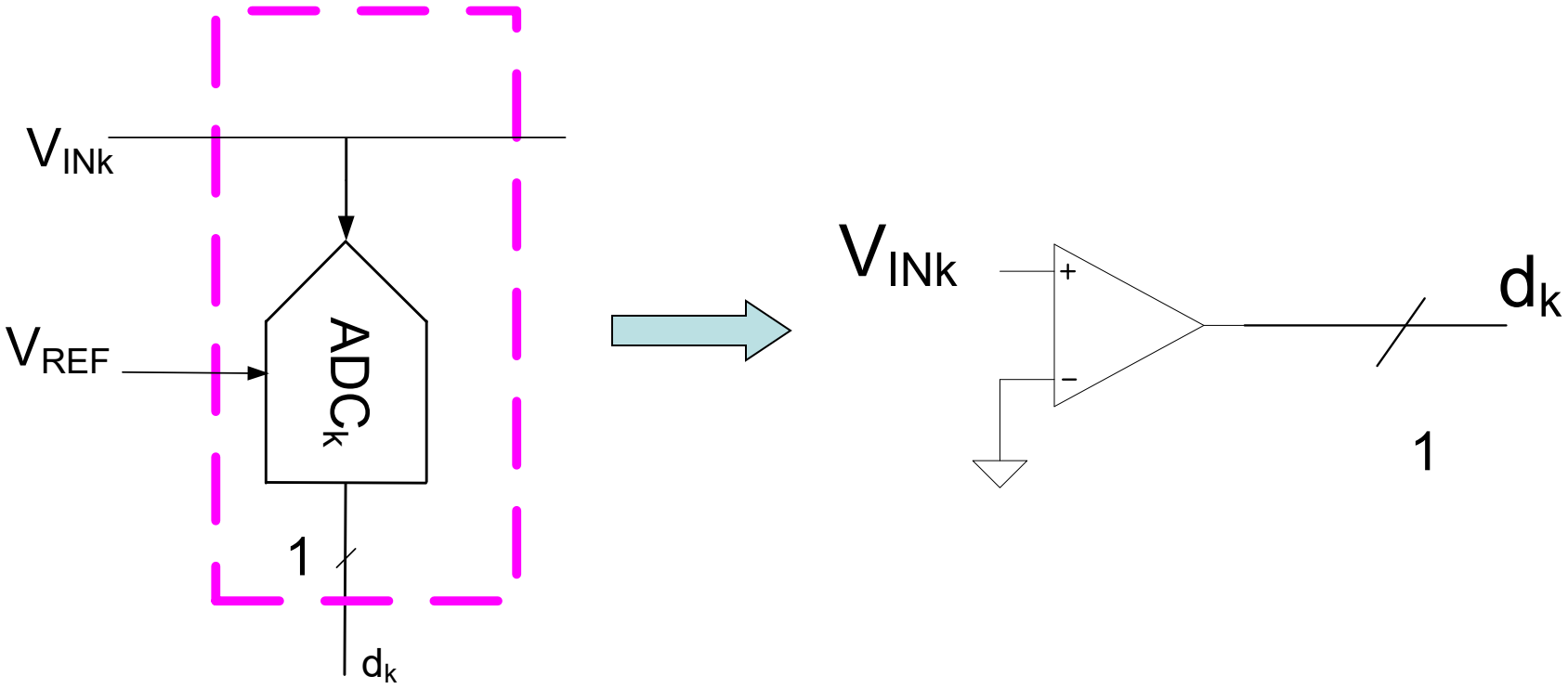
1-bit/Stage Pipeline Implementation



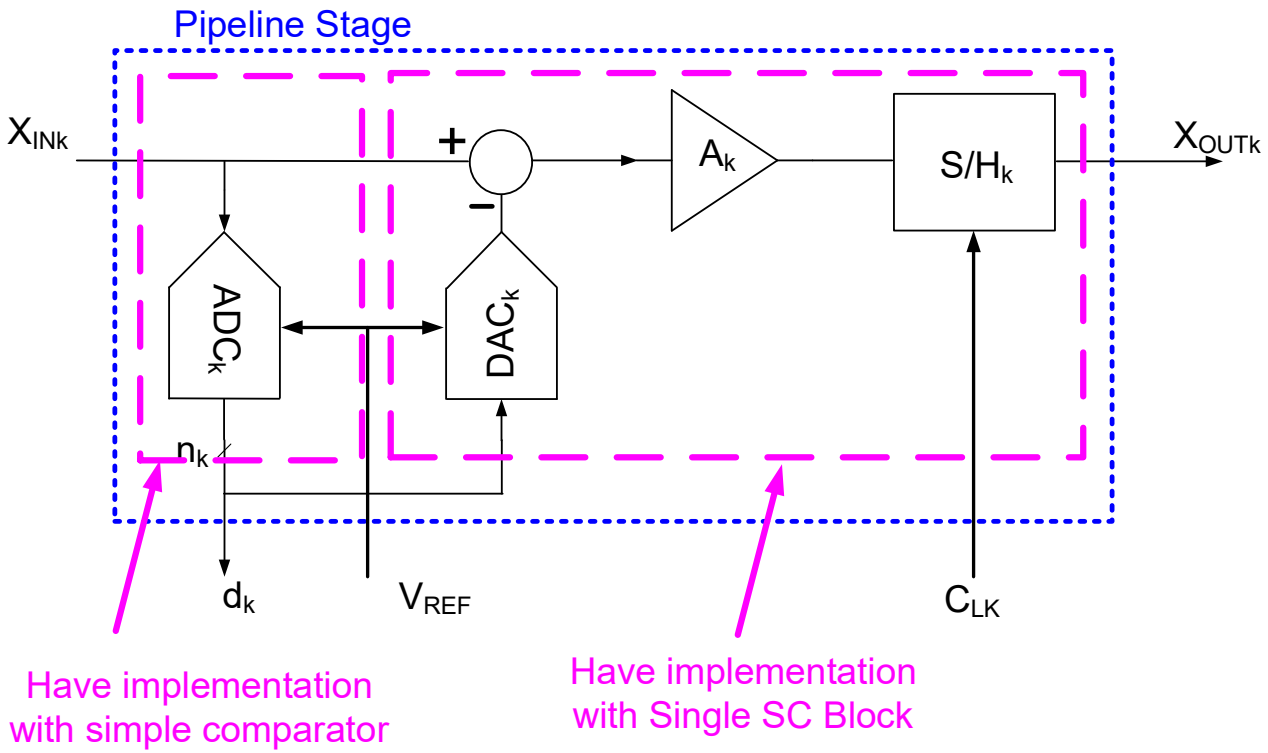


$$V_O = \begin{cases} 2V_{IN} + \dfrac{V_{REF}}{2} & V_{IN} < 0 \\ 2V_{IN} - \dfrac{V_{REF}}{2} & V_{IN} > 0 \end{cases}$$

1-bit/Stage Pipeline Implementation



Pipelined ADC Stage k

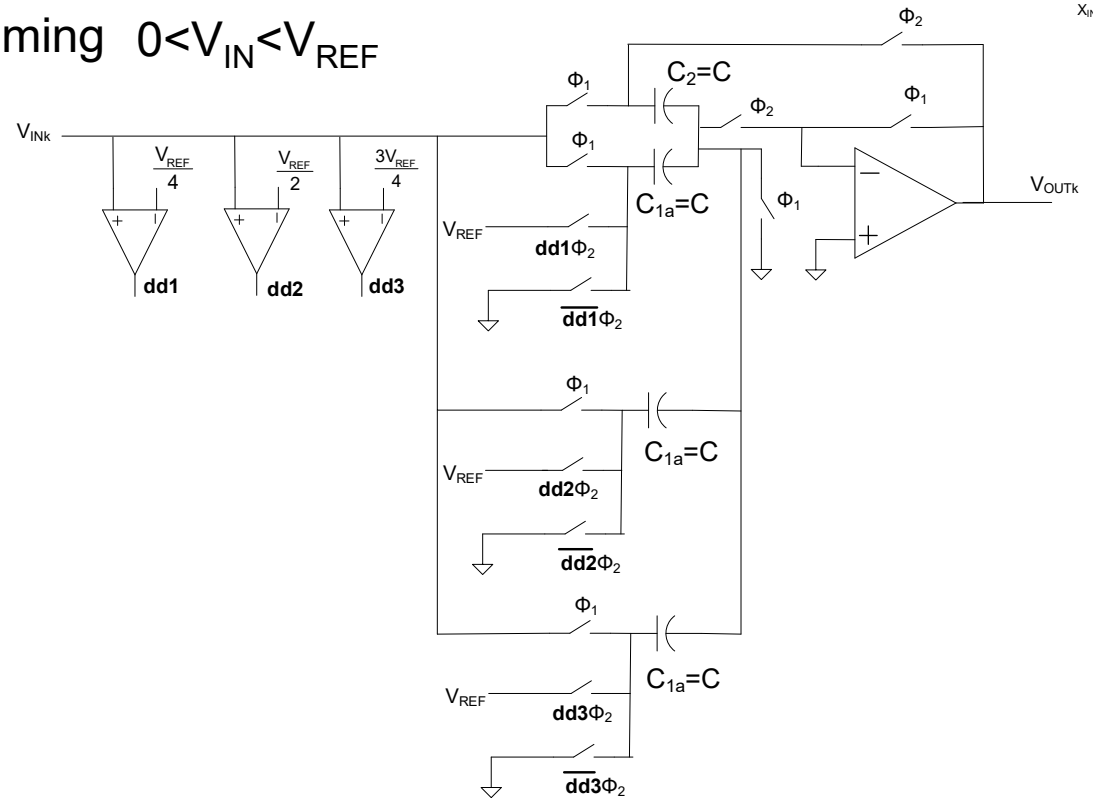


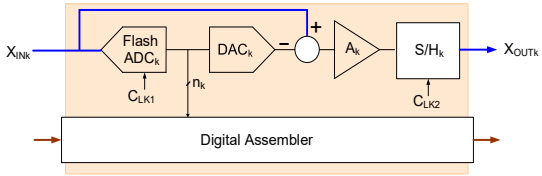
- Have shown simple implementation with 1-bit/stage structure
- Implementations with 2-bits/stage or 3-bits/stage also straightforward

Typical SC Pipeline Stage

For 2 bits/stage (Digital Assembler not shown)

Assuming $0<V_{IN}<V_{REF}$



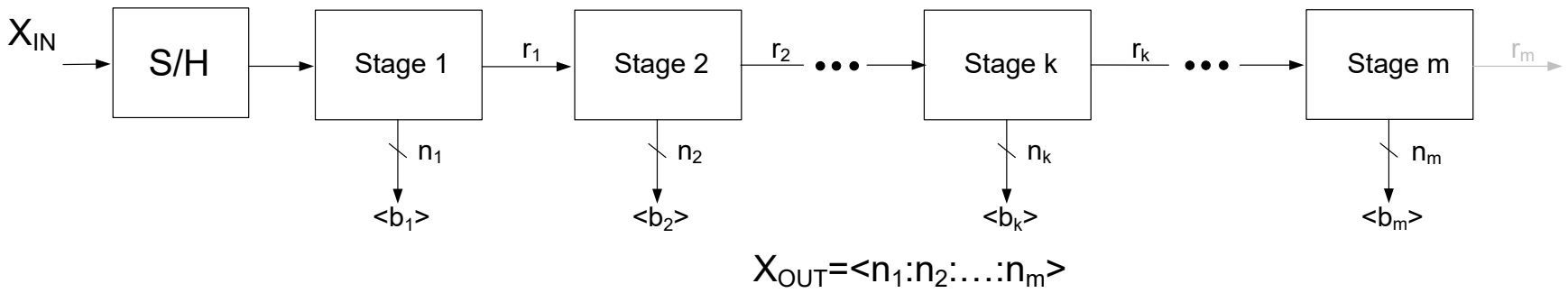


Gain =4

$$V_{OUT}=V_{IN}\left(1+\frac{C_{1a}+C_{1b}+C_{1c}}{C_2}\right)-\left(d_{d1}\left(\frac{C_{1a}}{C_2}\right)+d_{d2}\left(\frac{C_{1b}}{C_2}\right)+d_{d3}\left(\frac{C_{1c}}{C_2}\right)\right)V_{REF} \Rightarrow V_{OUTk}=4V_{INk}-\left(d_{dd1}+d_{dd2}+d_{dd3}\right)V_{REF}$$

- Directly use thermometer code outputs
- Can be extended to more bits/stage
- Accurate gain possible with good layout

Pipelined ADC



- Pipelined structure is widely used
- More than one bit/stage is often used
- Optimal number of bits/stage still an area of debate
- Conceptually can simply design one stage and then copy/paste to increase resolution
- Accuracy (and correspondingly power) in latter stages can be dramatically reduced
- Most power consumed in op amps
- Power dominantly allocated to S/H and MSB stages

ADC Types

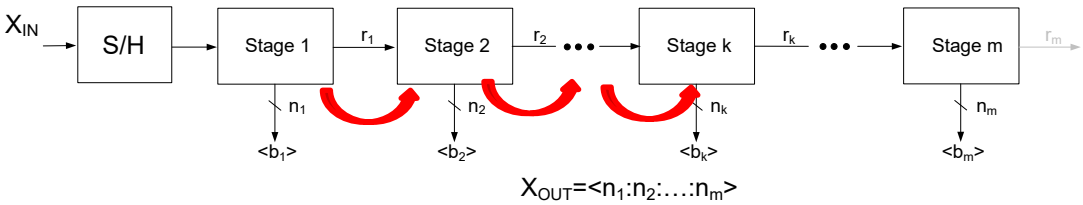
Nyquist Rate

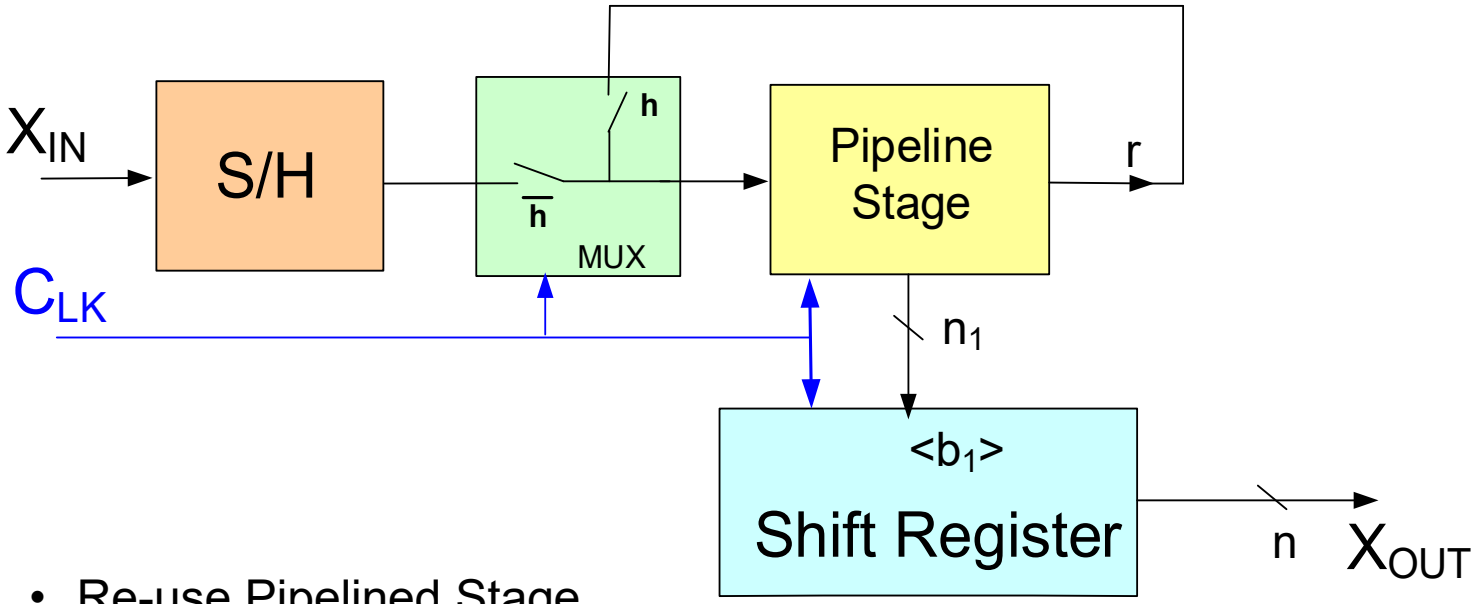
- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Interpolating
- Successive Approximation
- Folded
- Dual Slope

Over-Sampled

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

Cyclic (Algorithmic) ADC





- Re-use Pipelined Stage
- Small amount of hardware
- Effective thru-put decreases

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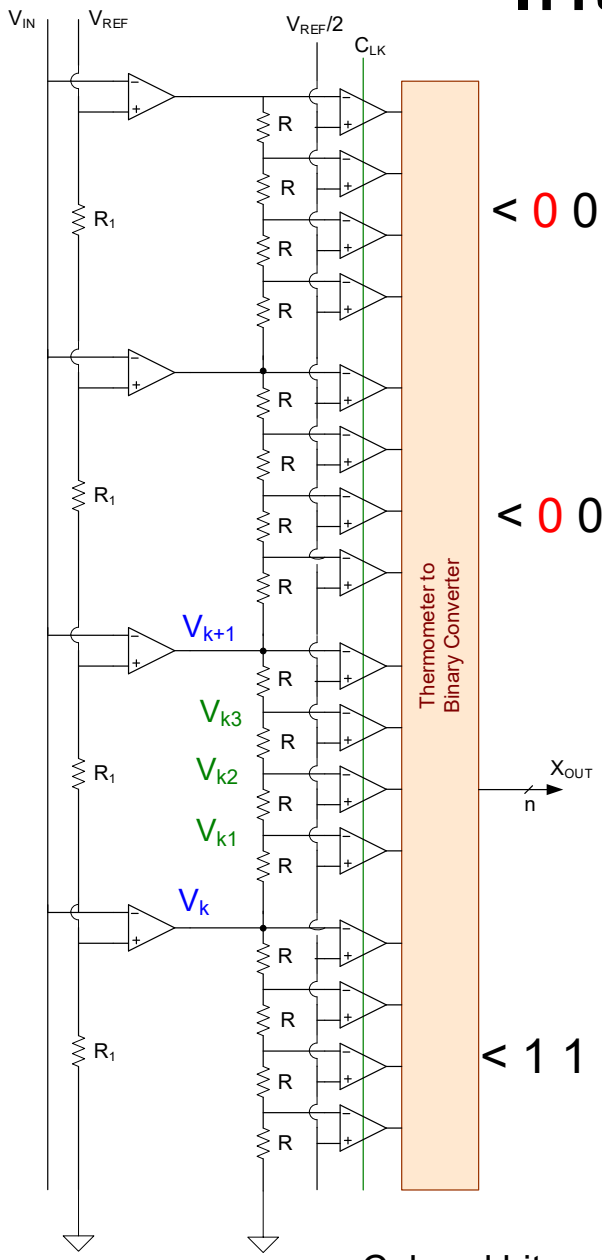
Interpolating ADC

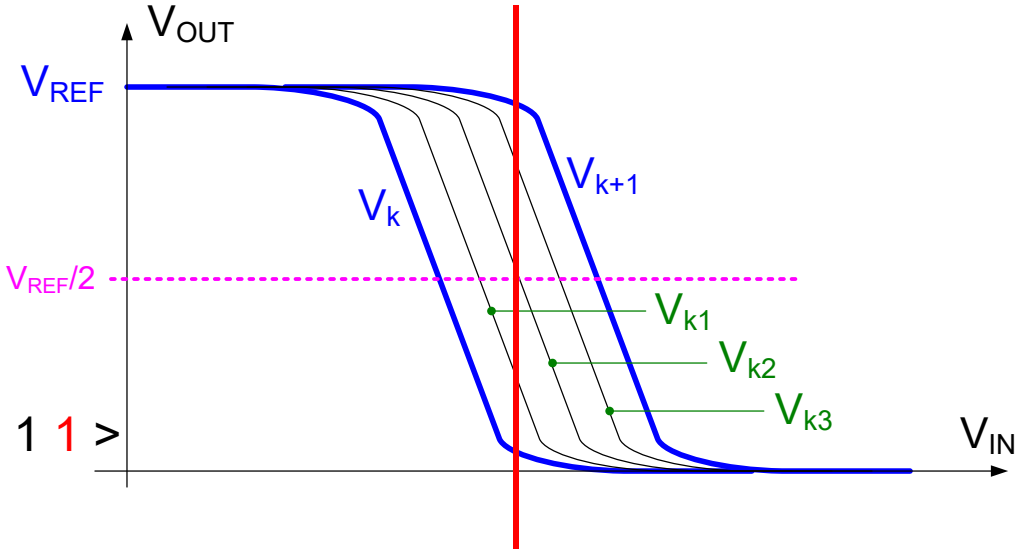


< 0 0 0 0 0 >

< 0 0 0 0 0 >

< 1 1 1 1 1 >

- Amplifiers are finite-gain saturating
- Amplifiers need not be accurate or linear
- Shown for 4-bit
- Same common-mode input on comparators
- Clocked comparators usually regenerative
- Reduces Offset Requirements for Comparators



< 1 1 0 0 0 >

Colored bits are shared

ADC Types

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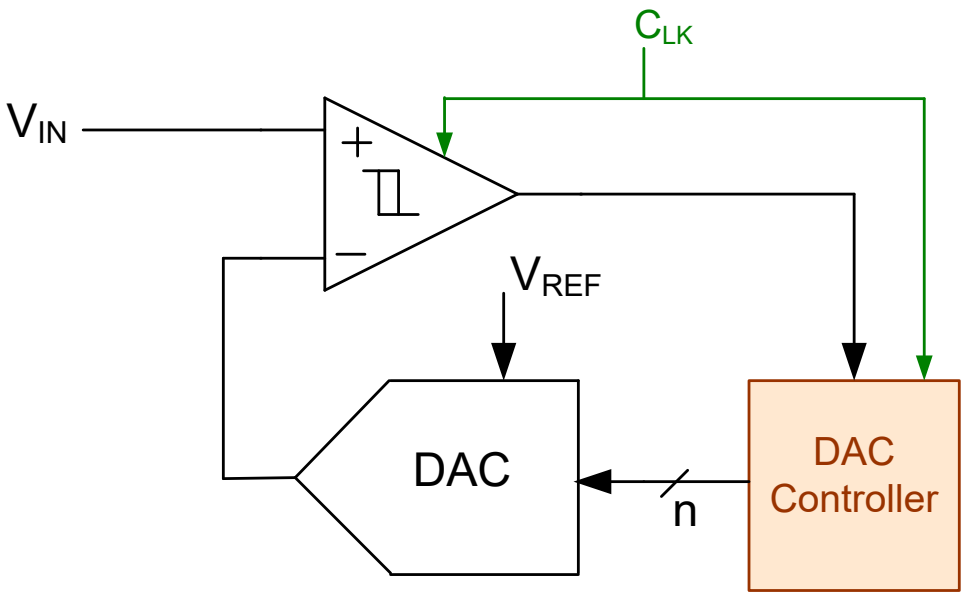
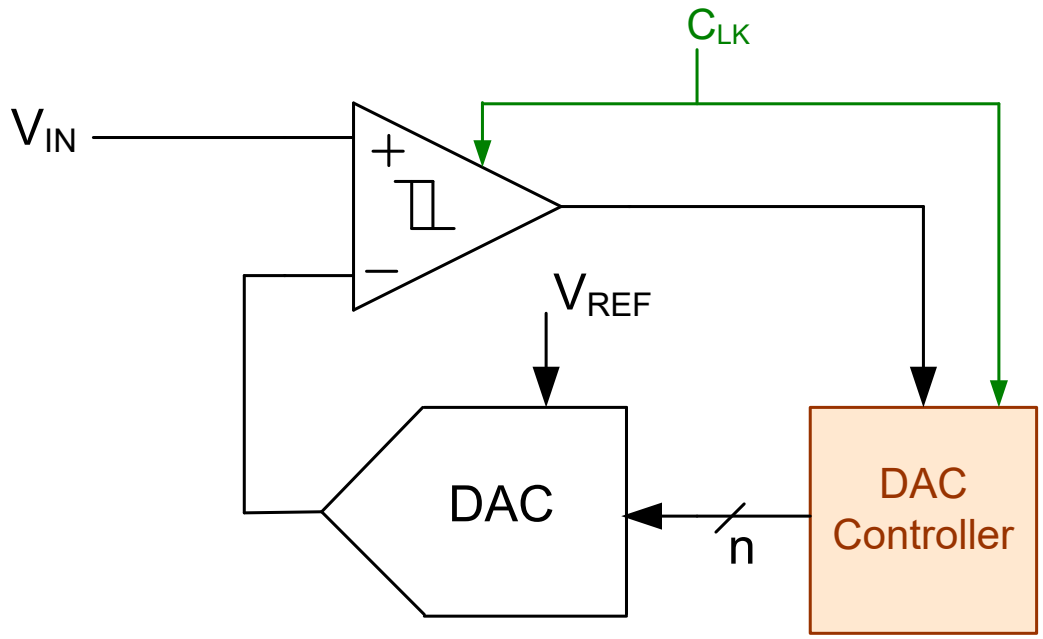
SAR ADC



ADCs
Texas Instruments

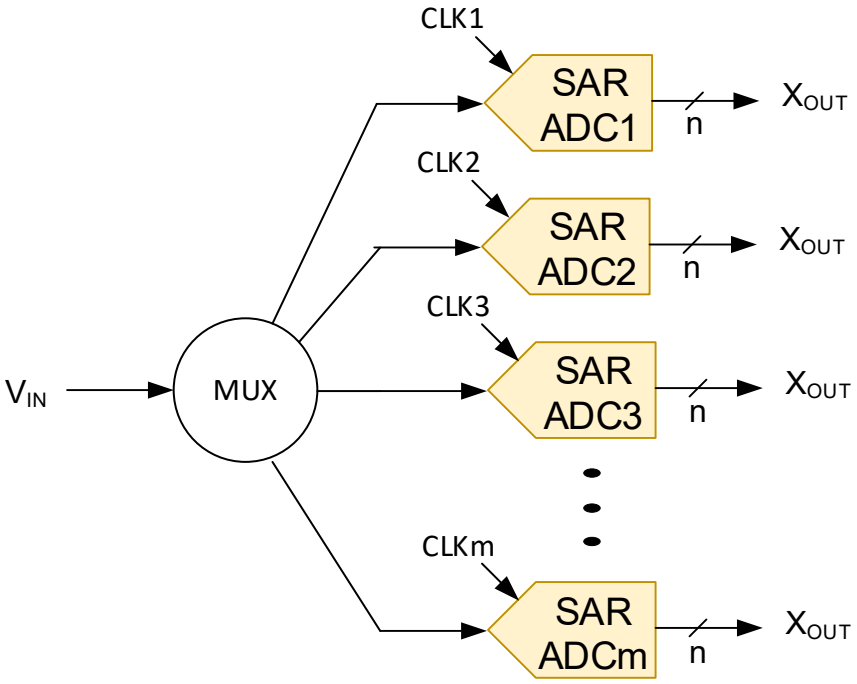
SAR		728
Pipeline		294
Delta Sigma		187
Folding Interpolating		66
Delta Sigma Modulator		9
Two-Step		6
Flash		3
Total		1293

SAR ADC

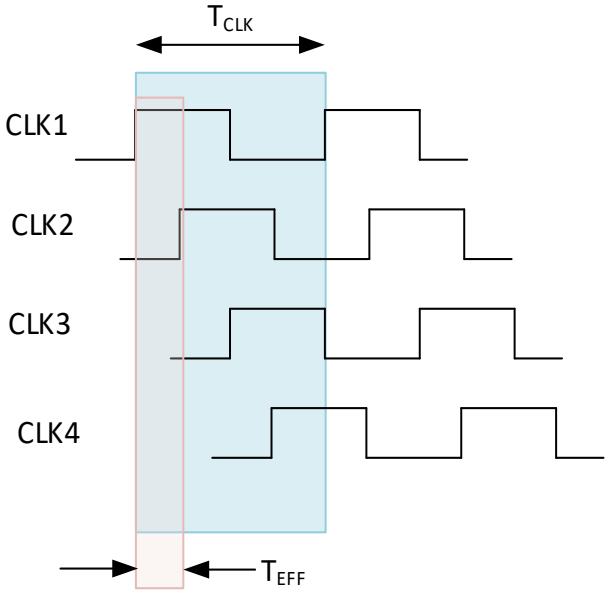


- DAC Controller may be simply U/D counter
- Binary search controlled by Finite State Machine is faster
- SAR ADC will have no missing codes if DAC is monotone
- Not very fast but can be small
- Any DAC can be used
- Single comparator !

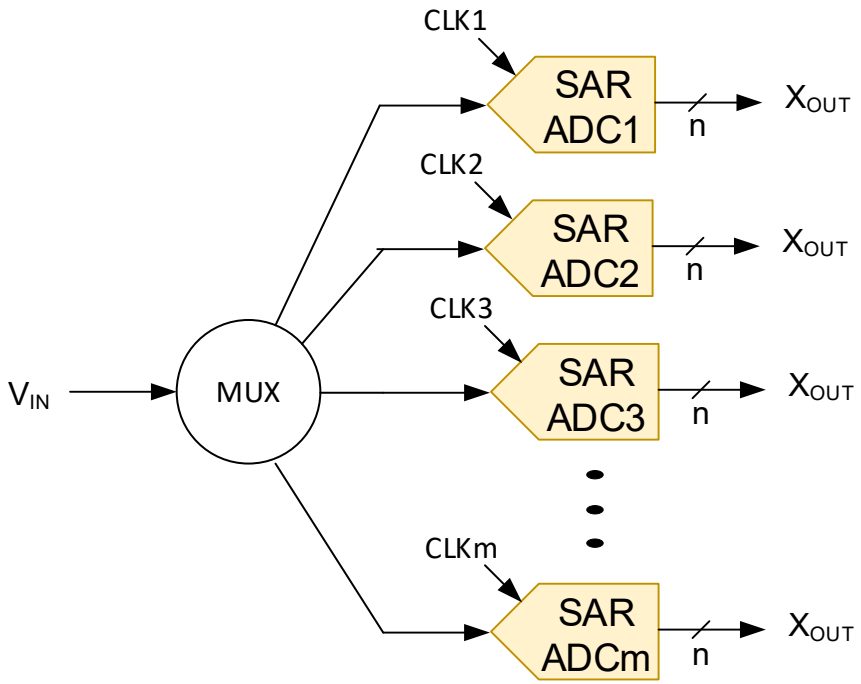
Time Interleaved SAR ADC



Time interleaving increases effective conversion rate by factor of m



Time Interleaved SAR ADC



- Provides high-speed solution when single SAR can not operate fast enough
- May be more energy efficient even if single SAR can work
- May provide better performance than pipelined structure
- Matching between stages is critical
- Clock phasing is critical
- Idea is 40+ years old but only recently has become popular
- Calibration is essential to provide matching and phasing

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- Multi-bit
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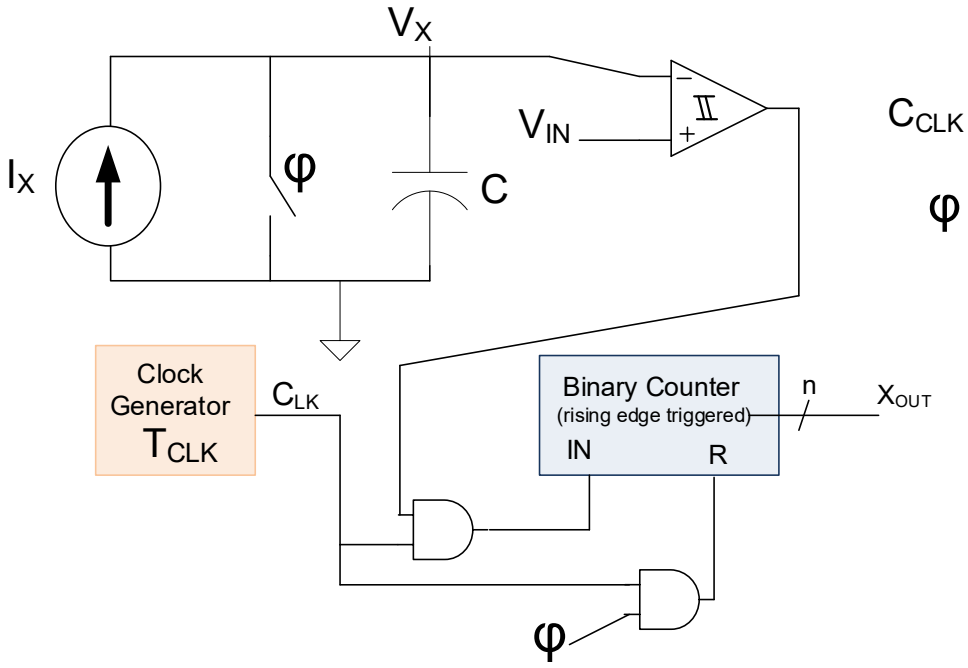
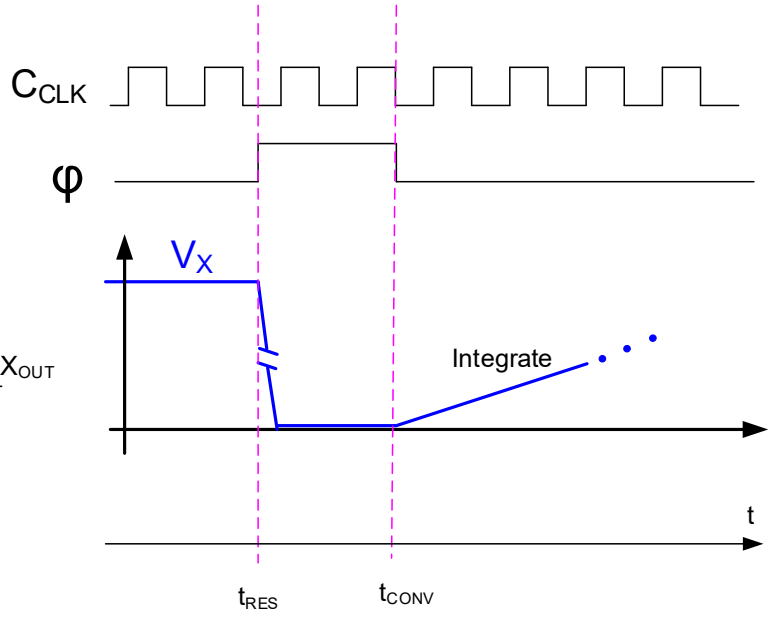
And Single Slope

Single-Slope ADC

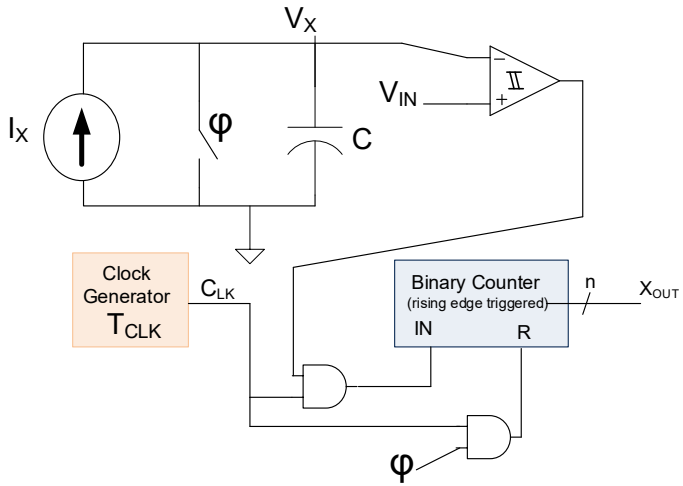
Sometimes Termed Integrating ADC





- Falling edge of φ synchronous with respect to falling edge of C_{LK}
- Can convert asynchronously wrt C_{CLK} or can be a clocked ADC where conversion clock signal is synchronous wrt C_{CLK}.
- Output valid when comparator output goes low
- Note V_{REF} not explicitly shown in ADC architecture
- Very simple structure if C is off-chip

Single-Slope ADC



Operation:

Assume $V_X(t_{CONV})=0$

$$V_X(t) = \frac{1}{C}\int_{t_{CONV}}^{t} I_X dt = \frac{I_X}{C}(t - t_{CONV}) \qquad (1)$$

Assume $I_X, V_{REF}, R, C, T_{CLK}$ are selected to satisfy the relationship

$$V_{REF} = \frac{1}{C}\int_{t_{CONV}}^{t_{CONV}+2^n T_{CLK}} I_X dt = \frac{I_X}{C} 2^n T_{CLK} \qquad \text{thus} \qquad V_{LSB} = \frac{V_{REF}}{2^n} = \frac{I_X}{C} T_{CLK} \qquad (2)$$

Comparator will stop counter when $V_X=V_{IN}$ and counter output will be $X_{OUT}=k$

thus $V_X(t_{CONV} + kT_{CLK}) = V_{IN} + \varepsilon$ where $0<\varepsilon<V_{LSB}$

It follows from (1) that

$$V_X(t_{CONV} + kT_{CLK}) = \frac{I_X}{C} kT_{CLK} = V_{IN} + \varepsilon \qquad (3)$$

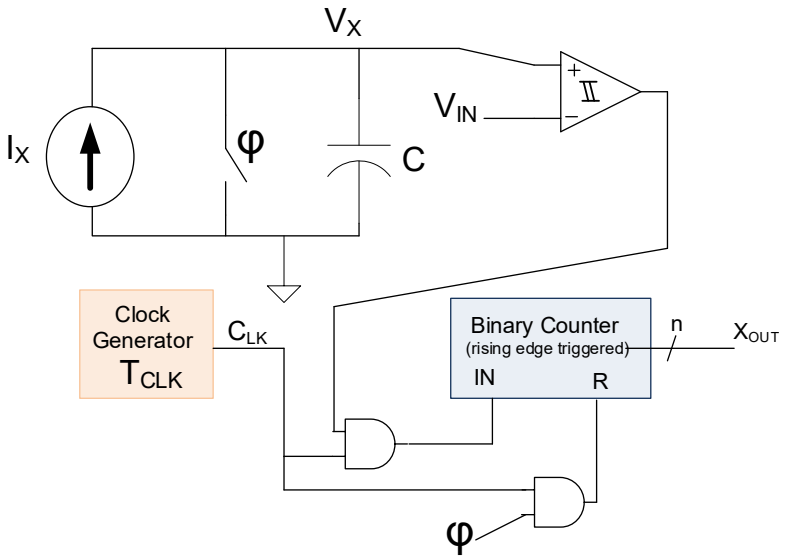
And finally from (2) and (3) that $V_{IN} = k\left(\frac{I_X}{C} T_{CLK}\right) - \varepsilon \cong \frac{k}{2^n} V_{REF}$

Single-Slope ADC

$I_X, V_{REF}, R, C, T_{CLK}$ must satisfy the relationship

$$V_{REF} = \frac{I_X}{C} 2^n T_{CLK} \qquad (1)$$

$$V_{IN} \cong \frac{k}{2^n} V_{REF}$$



Benefits: Very simple structure and can provide a low-cost easy solution for low speed applications

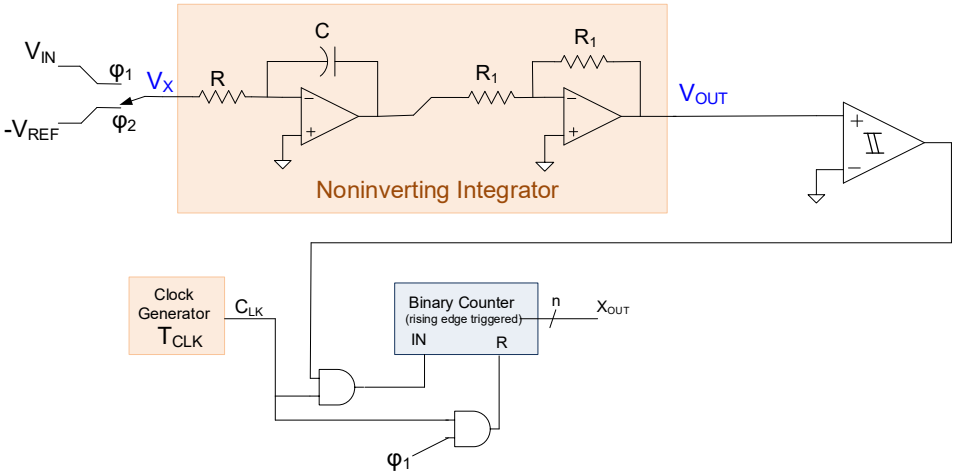
Limitations:

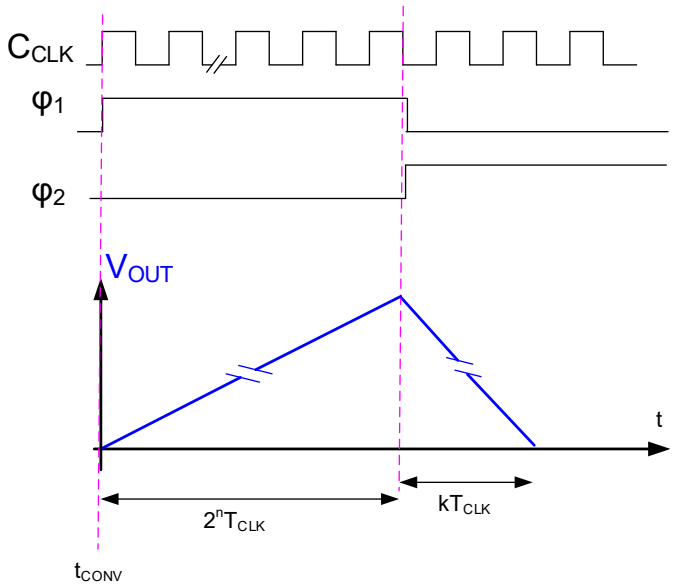
- Process variations make it difficult to satisfy (1)
- C is usually large and thus off chip is often most practical
- Linearity of C important (since often off-chip)
- Nonlinearity in I_X degrades performance
- R_{OUT} of I_X degrades performance
- Slow
- Not widely used

Options for improving performance:

- Introduce self-calibration cycle to satisfy (1) by trimming I_X or C
- Use high-impedance current source
- Use OP-Amp Based RC integrator

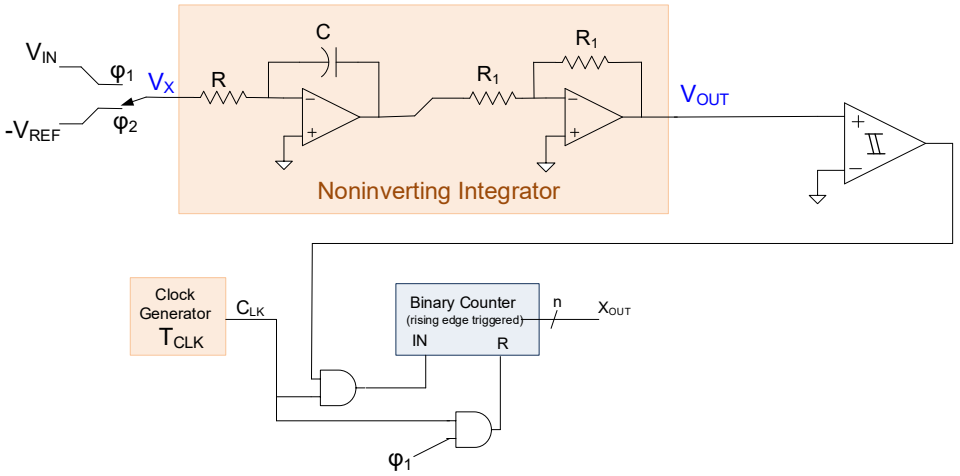
Dual-Slope ADC





- Output valid when comparator output transitions to Low
- Must set RC time constants and T_{CLK} so output does not saturate
- Shown as noninverting integrator but slight modification will also work with inverting integrator
- Other integrator structures could be used
- Can leave one or more clock cycles between integrate up and integrate down

Dual-Slope ADC



Operation:

$$V_{OUT}(t) = \frac{1}{RC}\int_{t_{CONV}}^{t} V_X dt$$

During φ_1, integrate V_{IN} for time $2^n T_{CLK}$

At end of integrate up interval, $$V_{OUT}\left(2^n T_{CLK}\right) = \frac{1}{RC} V_{IN} 2^n T_{CLK}$$

Reset counter at time $2^n T_{CLK}$

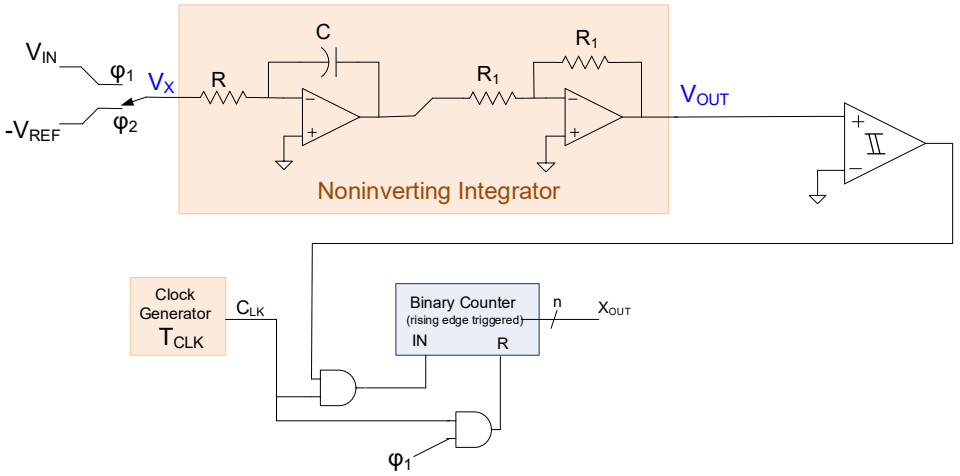
During φ_2, integrate $-V_{REF}$ until comparator goes low and count clock transitions during down integration interval. At time comparator changes states, $V_{OUT}=0$ and code in counter is k

$$0 = \frac{1}{RC}\int_{t_{CONV}}^{t_{CONV}+2^n T_{CLK}} V_{IN} dt - \frac{1}{RC}\int_{t_{CONV}+2^n T_{CLK}}^{t_{CONV}+2^n T_{CLK}+kT_{CLK}} V_{REF} dt \quad \Rightarrow \quad \frac{1}{RC} V_{IN} 2^n T_{CLK} = \frac{1}{RC} V_{REF} k T_{CLK}$$

Solving, obtain: $$V_{IN} = \frac{k}{2^n} V_{REF}$$

Dual-Slope ADC

$$V_{IN} = \frac{k}{2^n} V_{REF}$$



Observations:

Benefits

- Not dependent upon R, C, or T_{CLK} (provided integrator does not saturate)
- Very simple structure that can give good results and cost can be low
- Inherently monotone

Limitations:

- Capacitor large and likely must be off-chip
- Linearity of capacitor is important (particularly of concern when off-chip)
- Slow
- Not widely used

Stay Safe and Stay Healthy !

End of Lecture 39